DERWENT-ACC-NO:

2002-729483

DERWENT-WEEK:

200279

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TITLE:

Semiconductor device

INVENTOR: JUNG, J H

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 2000KR-0072134 (November 30, 2000)

PATENT-FAMILY:

PUB-NO

PUB-DATE

LANGUAGE PAGES

MAIN-IPC

KR 2002042312 A

June 5, 2002

N/A

001 H01L 021/76

APPLICATION-DATA:

PUB-NO

APPL-DESCRIPTOR

APPL-NO

APPL-DATE

KR2002042312A

N/A

2000KR-0072134

November 30, 2000

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: KR2002042312A

BASIC-ABSTRACT:

NOVELTY - A semiconductor device prevents etching of a shallow trench isolation

(STI) layer and improves step coverage of the STI layer by using an automatic

layer deposition boron nitride (ALD-BN) or plasma enhanced boron nitride

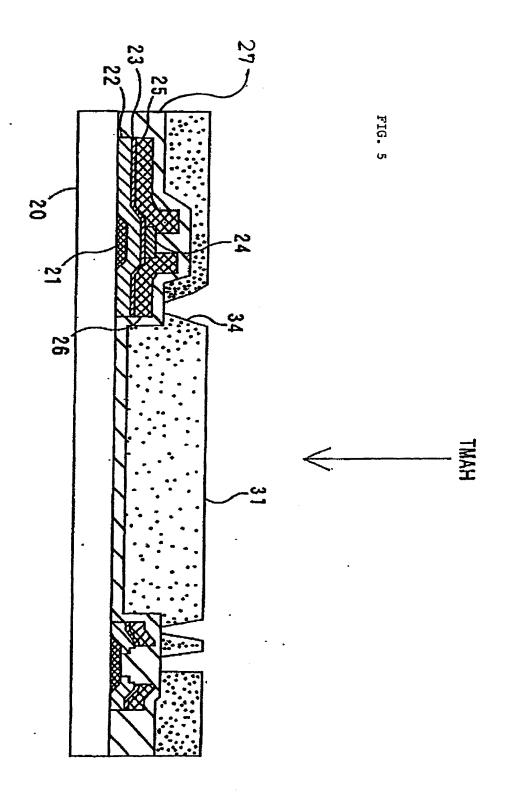
(PE-BN) as an insulating layer.

DETAILED DESCRIPTION - A semiconductor device comprises a substrate (50)

including an adequately aligned STI layer (56) having a groove (g) around the

outer edge portion, an insulating part (64b) in the groove

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of the STI layer,

sidewall spacers (64a) of a gate electrode (60) located at a defined portion of

the substrate, junction areas (68) formed on both sides of the gate electrode

and the sidewall spacers in the substrate, an interlayer dielectric (72)

covering the resultant substrate, an etch stopper (70) located between the

resultant substrate and the interlayer dielectric, and a metal interconnection

(74) formed in the interlayer dielectric and connected with a defined portion

of the junction areas. At this point, the insulating part and sidewall spacers

comprise the same material, i.e. ALD-BN or PE-BN.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: SEMICONDUCTOR DEVICE

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C12B;

EPI-CODES: U11-A08; U11-C01; U11-C07; U11-C08A2;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2002-206634

08/05/2003, EAST Version: 1.04.0000

